Notice of Allowability	Application No.	Applicant(s)	
	10/782,461	MILLER ET AL.	
	Examiner	Art Unit	
	Nitin Patel	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/23/2006*.

2. ☒ The allowed claim(s) is/are *1-44*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Nitin Patel

REASON FOR ALLOWANCE

1. Claims 1-44 is allowed.

2. The following is an examiner's statement of reason for allowance:

The prior art fails to teach or suggest a display driver comprising a single chip including: a plurality of display outputs each for outputting a drive voltage to a row or a column of a display; and a plurality of configuration bits each having a row/column setting, wherein each configuration bit is exclusively associated with one or more of said plurality of display outputs such that said row/column setting of said configuration bit is used to configure all of said associated one or more display outputs for driving either rows or columns of the display as claimed in claim 1.

The prior art fails to teach or suggest a display driver comprising a single chip including: a plurality of driver blocks, each of said plurality of driver blocks having: a plurality of display outputs each for outputting a drive voltage to a row or column of a display; and a configuration bit having a row/column setting, wherein said driver block is configured to drive either rows or columns of the display according to said configuration bit row/column setting, and each of said plurality of display outputs of said driver block is thereby configured to input said drive voltage to either a row or a column of the display, respectively as claimed in claim 7.

The prior art fails to teach or suggest a display driver comprising a single chip including: a first driver block having: a plurality of display outputs, each for outputting a drive voltage to either a row or a column of a display; and a configuration bit having a row/column setting for setting said first driver block to drive either rows or columns of

the display, wherein all of said plurality of display outputs are set to drive either rows or columns of the display, respectively; and a second driver block including: another plurality of display outputs, each for outputting a drive voltage to either a row or a column of the display; and another configuration bit having a row/column setting for setting said second driver block to drive either rows or columns of the display, wherein all of said another plurality of display outputs are set to drive either rows or columns of the display, respectively as claimed in claim 13.

The prior art fails to teach or suggest a display driver for driving a bistable display, said display driver comprising a single chip including: a plurality of driver blocks, each driver block including: a plurality of display outputs, each for outputting a voltage to a row or a column of a display; and a configuration bit having a row/column setting, wherein all of said plurality of display outputs of said driver block are set to drive either rows or columns of the display according to said configuration bit setting, wherein each of said plurality of driver blocks can be set independently to drive either rows or columns, and further wherein said driver is adapted to drive a bistable display as claimed in claim 19.

The prior art fails to teach or suggest a display driver comprising a single chip including: a plurality of driver blocks, each driver block having a corresponding plurality of display outputs, each of said plurality of display outputs being effective for outputting a voltage to a row or a column of a display; and a plurality of configuration bits equal to the number of said plurality of driver blocks, wherein each configuration bit has a row/column setting and is associated with a corresponding driver block, and further

wherein, each driver block is set to drive either rows or columns according to said row/column setting, such that each of said corresponding plurality of display outputs of said driver block are all set for driving a row or a column, respectively, of the display as claimed in claim 27.

The prior art fails to teach or suggest a display driver for driving a display, said display driver comprising a single chip including: a plurality of driver blocks, each driver block including: a plurality of display outputs, each for outputting a voltage to a row or a column of a display; a configuration bit having a row/column setting; a cascade input; and a cascade output, wherein all of said plurality of display outputs of said driver block are set to drive either rows or columns of the display according to said configuration bit setting, wherein each of said plurality of driver blocks can be set independently to drive either rows or columns, and further wherein two or more of said plurality of driver blocks can be cascaded together for driving additional rows or columns of the display by connecting a cascade input of one of said two or more driver blocks to the cascade output of another of said two or more driver blocks as claimed in claim 28.

The prior art fails to teach or suggest a display driver comprising a single chip including: a plurality of display outputs each for outputting a drive voltage to a row or a column of a display; a configuration bit having a row/column setting; a cascade input; and a cascade output, wherein the row/column setting of said configuration bit is used to configure one or more display outputs for driving either a row or a column of the display, and further wherein a first display driver can be cascaded with a second display driver by connecting the cascade output of the first display driver with the cascade input

of the second display driver for driving additional rows or columns of the display as claimed in claim 30.

The prior art fails to teach or suggest a liquid crystal display device comprising: chiral nematic liquid crystal material; substrates that form therebetween a region in which said liquid crystal material is disposed, wherein said substrates cooperate with said liquid crystal material to form in said region scattering focal conic and reflecting planar textures that are stable in the absence of an electric field; electrodes disposed on said substrates effective to apply an electric field to areas of said region corresponding to a plurality of columns and rows; wherein incident light travels in a direction through said region, comprising a light absorbing back layer disposed downstream of said region relative to said direction of incident light; and a display driver for applying an electric field for transforming at least a portion of said liquid crystal material to at least one of the focal conic and planar textures, said display driver comprising a single chip including: a plurality of display outputs each for outputting a drive voltage to one of said rows or one of said columns; and a plurality of configuration bits each having a row/column setting; wherein each said configuration bit is exclusively associated with one or more of said plurality of display outputs such that said row/column setting of said configuration bit is used to configure all of said associated one or more display outputs for driving either said rows or said columns as claimed in claim 31.

The prior art fails to teach or suggest a reflective full color liquid crystal display device comprising: first chiral nematic liquid crystal material comprising liquid crystal having a pitch length effective to reflect visible light of a first color, second chiral nematic

liquid crystal material comprising liquid crystal having a pitch length effective to reflect visible light of a second color, and third chiral nematic liquid crystal material comprising liquid crystal having a pitch length effective to reflect visible light of a third color; substrates that form therebetween a first region in which said first material is disposed, a second region in which said second material is disposed and a third region in which said third material is disposed, wherein said first region, said second region and said third region are stacked relative to each other; electrodes disposed on said substrates effective to apply an electric field to areas of said first region, said second region and said third region, corresponding to a plurality of columns and rows; wherein said substrates cooperate with said first material, said second material and said third material to form in said first region, said second region and said third region, scattering focal conic and reflecting planar textures that are stable in the absence of an electric field; wherein incident light travels in a direction sequentially through said first region, said second region and said third region, said first region being closest to a viewer, comprising a light absorbing back layer disposed downstream of said third region relative to said direction of incident light; wherein the incident light is reflected by the planar textures of said first region, said second region and said third region such that reflected light leaving the display exhibits a color that is an additive mixing of combinations of said colors which are reflected from said planar textures, and said incident light passing through said first region, said second region and said third region is absorbed by said light absorbing back layer; and a display driver for applying an electric field for transforming at least a portion of the liquid crystal of at least one of said

first material, said second material and said third material, to at least one of the focal conic and planar textures, said display driver comprising a single chip including: a plurality of display outputs each for outputting a drive voltage to one of said rows or one of said columns, and a plurality of configuration bits each having a row/column setting, wherein each said configuration bit is exclusively associated with one or more of said plurality of display outputs such that said row/column setting of said configuration bit is used to configure all of said associated one or more display outputs for driving either said rows or said columns; wherein a proportion of at least one of said first material, said second material and said third material exhibits a planar texture in the absence of an electric field and a proportion of the at least one of said first material, said second material and said third material exhibits a focal conic texture in the absence of an electric field, wherein said display driver provides an electric field pulse of sufficient amplitude and duration to change the proportions of the at least one of said first material, said second material and said third material in said planar and focal conic textures, whereby the intensity of light reflected may be selectively adjusted as claimed in claim 34.

The prior art fails to teach or suggest a reflective liquid crystal display device comprising: first chiral nematic liquid crystal material comprising liquid crystal having a pitch length effective to reflect electromagnetic radiation of a first wavelength and second chiral nematic liquid crystal material comprising liquid crystal having a pitch length effective to reflect electromagnetic radiation of a second wavelength; substrates that form therebetween a first region in which said first material is disposed and a

second region in which said second material is disposed, wherein said first region and said second region are stacked relative to each other; electrodes disposed on said substrates effective to apply an electric field to areas of said first region and said second region, corresponding to a plurality of columns and rows; wherein said substrates cooperate with said first material and said second material to form in said first region and said second region, scattering focal conic and reflecting planar textures that are stable in the absence of an electric field; wherein incident light travels in a direction sequentially through said first region and said second region, said first region being closest to a viewer, comprising a light absorbing back layer disposed downstream of said second region relative to said direction of incident light; wherein the incident light is reflected by the planar textures of said first region and said second region such that reflected light leaving the display exhibits a wavelength that is an additive mixing of combinations of said wavelengths which are reflected from said planar textures, and said incident light passing through said first region and said second region is absorbed by said light absorbing back layer; and a display driver for applying an electric field for transforming at least a portion of said liquid crystal material of the liquid crystal of at least one of said first material and said second material, to at least one of the focal conic and planar textures, said display driver comprising a single chip including: a plurality of display outputs each for outputting a drive voltage to one of said rows or one of said columns, and a plurality of configuration bits each having a row/column setting, wherein each said configuration bit is exclusively associated with one or more of said plurality of display outputs such that said row/column setting of said configuration bit is

used to configure all of said associated one or more display outputs for driving either said rows or said columns; wherein a proportion of at least one of said first material and said second material exhibits a planar texture in the absence of a field and a proportion of the at least one of said first material and said second material exhibits a focal conic texture in the absence of an electric field, wherein said display driver provides an electric field pulse of sufficient amplitude and duration to change the proportions of the at least one of said first material and said second material in said planar and focal conic textures, whereby the intensity of light reflected may be selectively adjusted as claimed in claim 35.

The prior art fails to teach or suggest a chiral nematic liquid crystal display, comprising: chiral nematic liquid crystal material located between first and second substrates, said material including a planar texture having a circular polarization of a predetermined handedness and a focal conic texture that are stable in an absence of an electric field; electrodes disposed on said first and second substrates effective to apply an electric field to areas of said region corresponding to a plurality of columns and rows; a first quarter wave retarder located adjacent to said first substrate; a linear polarizer located adjacent to said first quarter wave retarder; a second quarter wave retarder located adjacent to said linear polarizer; a transflector having a reflective side adjacent to said second quarter wave retarder and a light transmitting side; a light source adjacent to said transmitting side, said light source being selectively energizeable to emit light through said transflector; and a display driver for applying an electric field for transforming at least a portion of said liquid crystal material to at least one of the focal

conic and planar textures, said display driver comprising a single chip including: a plurality of display outputs each for outputting a drive voltage to one of said rows or one of said columns; and a plurality of configuration bits each having a row/column setting, wherein each said configuration bit is exclusively associated with one or more of said plurality of display outputs such that said row/column setting of said configuration bit is used to configure all of said associated one or more display outputs for driving either said rows or said columns as claimed in claim 38.

The prior art fails to teach or suggest a liquid crystal display device comprising: chiral nematic liquid crystal material; substrates that form therebetween a region in which said liquid crystal material is disposed; at least one alignment surface that is effective to substantially homogeneously align the liquid crystal director adjacent thereto, wherein at least one of said substrates and each said alignment surface cooperates with said liquid crystal material so as to form focal conic and planar textures that are stable in the absence of an electric field, each said alignment surface being effective to provide at least one of the following: (a) a brightness at a wavelength of peak reflection of said planar texture that is increased by at least 5% as compared to an identical liquid crystal device but with inhomogeneous alignment surfaces, (b) the focal conic texture with a reflectance that does not exceed 10% of electromagnetic radiation incident on the display device at a wavelength of peak reflection of the planar texture, and (c) a degree of circular polarization at a wavelength of peak reflection of the planar texture, which is increased by at least 10% as compared to an identical liquid crystal device but with inhomogeneous alignment surfaces; and a display driver for applying an

electric field for transforming at least a portion of said liquid crystal material to at least one of the focal conic and planar textures, said display driver comprising a single chip including: a plurality of display outputs each for outputting a drive voltage to one of said rows or one of said columns; and a plurality of configuration bits each having a row/column setting, wherein each said configuration bit is exclusively associated with one or more of said plurality of display outputs such that said row/column setting of said configuration bit is used to configure all of said associated one or more display outputs for driving either said rows or said columns as claimed in claim 39.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H. Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nitin Patel
Examiner
Art Unit 2629